



Mining your own expertise



Magillem IP-XACT Packager

Description

Moving efficiently to an IP based methodology and flow requires legacy IP libraries to be captured in a technology independent format with an easy-to-use, scalable and automated process. Magillem IP Packager automatically creates an IP-XACT certified description for any VHDL, Verilog or SystemC component using a technology that is non-intrusive to your existing flow. The packager scalability enables automatic import of legacy component libraries and its high level of modularity allows it to integrate with any client directory structure and to handle customer specific information. Magillem IP-XACT packager advantages are:

- ✓ Non intrusive, scalable and automatic process for legacy and new IPs.
- ✓ Proven methodology enabling seamless packaging of IP client portfolio.
- ✓ Support any kind of IP description, client data structure and input information, through a highly customizable process.
- ✓ The packager scalable architecture also enables it to automatically re-capture a library of components following input changes.
- ✓ Support of all IP-XACT formats.
- ✓ IP-XACT compliance and data consistency ensured by construction and assessed through the robust Magillem IP-XACT checkers suite.
- ✓ CAD flow independence.

Features

As a major Contributing Member of the Spirit Consortium, Magillem has a proven experience with IP-XACT usage. Magillem IP Packager can target any IP-XACT version:

- Legacy IP-XACT versions: 1.0, 1.1, 1.2, 1.4 and 1.5;
- IEEE1685 standard.

Magillem Packager relies on the Magillem Compliance Checkers Suite that guarantees the validity of generated files against IP-XACT grammar, semantics and the Spirit Consortium guidelines. Magillem Packager is able to abstract files from the following formats:

- VHDL IEEE 1076 : '87, '93.
- Verilog IEEE 1364 : '95, '01, '05.
- SystemC IEEE 1666 : 1.x, 2.x, TLM 1.x, TLM 2.x.
- Any CSV or Excel spreadsheet can be imported with a GUI, assisting the translation to/from IP-XACT

The Magillem Packager is able to package hierarchical components across many libraries, containing a mix of VHDL and Verilog instances, and create the corresponding IP-XACT file set.

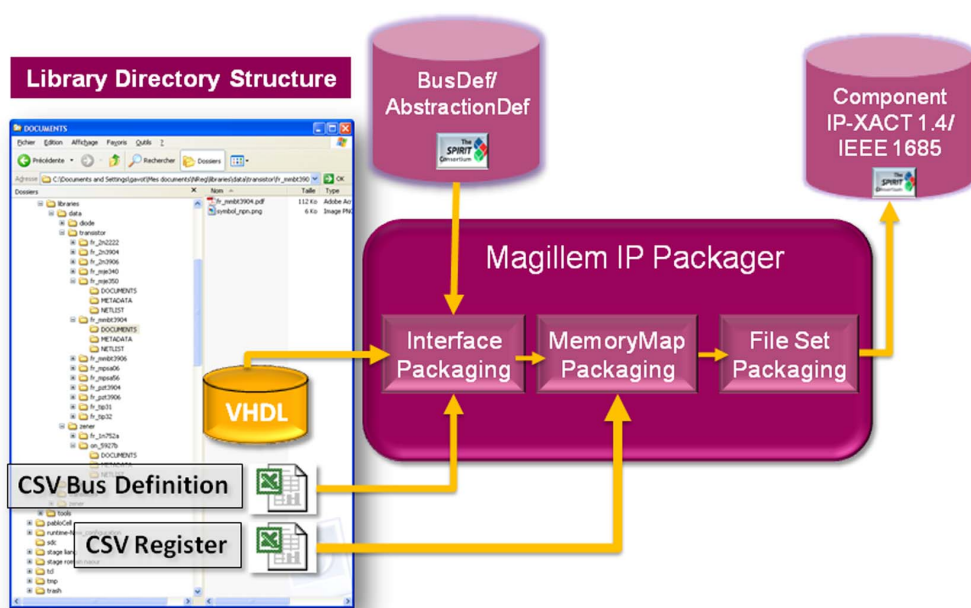
The following language extensions are also supported, with Magillem AMS Solution:

- VHDL-AMS : IEEE 1076.1
- Verilog-AMS : LRM 2.3.1
- SystemC-AMS: LRM 1.0.

Services proposed by Magillem Design Services on IP Packaging are:

- Audit of the existing libraries, and definition of the most efficient import strategy.
- Tool customization to handle the customer specific information and integrating with the client infrastructure.

Architecture



Magillem IP Packager can plug to various client infrastructures:

- Directory structure:
 - Any CoReUse version.
 - Client specific structure.
- IP Yellow Pages integration;
- Direct links to versioning control systems: CVS, SVN, ClearCase.

Benefits

To the HW System architect Engineer:

- Fast architecture Exploration and definition

To the IP provider:

- Package IP in a reusable format that will guide the IP integrator through the configuration, implementation, and verification

To the IP integrator:

- Heterogeneous architecture integration
- Easy configurable and reusable IP library management
- Auto Generation of ESL/HDL code

To the Project lead:

- Synchronization of collaborative work, verification, tracking, reporting

To the verification Engineer:

- Fast verification of the HW implementation of IP
- Validation plan and coverage scoring
- Easy monitoring, configuration and initialization

“If I'd known how much packing I'd have to do, I'd have run again”

Harry S. Truman



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Specifications

| MIP FEATURES | Premium | Platinum |
|---|---------|----------|
| IP-XACT v1.0, v1.2, v1.4, v1.5 certified | X | X |
| IP-XACT IEEE 1685 | X | X |
| Coherency Check | X | X |
| Source of importation | | |
| CoreUse standard structure of repository support | X | X |
| Custom structure of repository support | X | X |
| IP yellow Page integration | X | X |
| Hierarchical IPs containing a mix of VHDL and Verilog components | X | X |
| Complete File set creation of the component and its dependencies | X | X |
| Change and release management tool | | |
| CVS connector | X | X |
| Clearcase connector | X | X |
| Standard digital and Analog HDL import | | |
| VHDL IEEE 1076, '83 or '93 import | X | X |
| Verilog IEEE 1364, '95, '01 or '05 import | X | X |
| SystemC IEEE 1666 import | | X |
| VHDL-AMS IEEE 1076.1 import | | X |
| Verilog-AMS LRM 2.3.1 import | | X |
| SystemC-AMS LRM 1.0 import | | X |
| Customer Specific information Import | | |
| Register and memory map definition: CSV, Excel, Framemaker, SystemRDL | X | X |
| Legacy XML | X | X |
| Documentation | X | X |

Email: contact@magillem.com
 Web: www.magillem.com

USA

Magillem
 161 West 54th street suite #202A
 New york, NY 10019 USA
 Tel: +1 212-378-4409
 Fax: +1 212-292-3999

Europe

Magillem
 4 rue de la pierre Levée
 75011 Paris, France
 Tel : +33. (0)1.40.21.35.50
 Fax : +33. (0)1.53.36.75.08

Asia

Shinagawa Intercity Tower A, Level
 28, Shinagawa Intercity A
 2-15-1 Kounan Minato-ku
 Tokyo, Japan 108-6028
 Tel : +81 3 6717 4589
 Tel : +81 90 4748 1652