



Magillem Platform Assembly

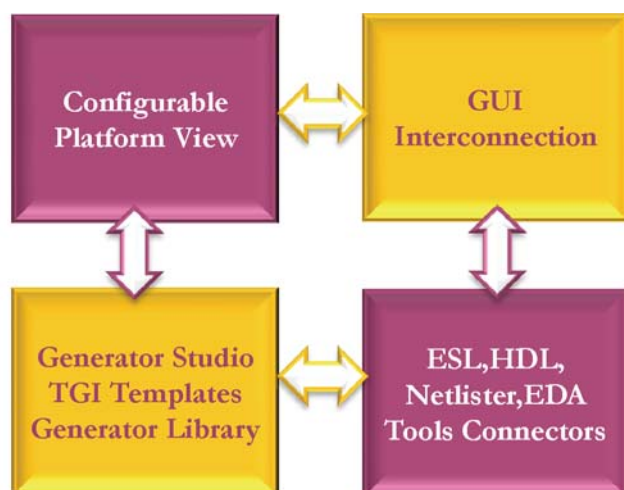
Description

To accelerate the design of complex systems, such as System-on-Chip (SoC), and FPGA based solutions, the IP-XACT standard provides a mechanism for describing and handling multi-sourced IP that enables automated design integration and configuration within multi-vendor tool flows.

To achieve these goals, Magillem present MPA the center piece of a powerful intuitive, Integrated Design Environment. The user friendly interface guides the designer during platform assembly and configuration, and streamlines exploration and implementation of IP-based systems:

- A complete graphical platform editor providing advanced parameterization, reusable methodology and collaborative features
- A digital and/or analog design environment (editor, DRC, library management)
- A set of predefined automated operations to easily connect IP through the hierarchy, handle components (move, merge, flat, insert...) and reduce risks of errors.
- A support of virtual hierarchy allowing the same platform to be hierarchically described according the flow step (power domain, verification, software, team, abstraction level, ...).
- A graphical interface to manage the library of generator, plugins for the Magillem Generator Studio and customize the automation of the platform for dedicated applications
- A large range of connectors to EDA tools (Mentor, Cadence, Synopsys, Xilinx, Altera)
- RTL and ESL netlister (VHDL, Verilog, SystemC, VHDL-AMS, Verilog-A, SystemC-AMS)
- Automated generation of an environment used for verification, integrated with a cockpit to control and monitor the Design Under Test, in order to manage the progress.

MPA is well adapted for the V-cycle methodology used by multi-site design teams. Using a top-down approach, it builds a complete view of the system, with all interconnections, ready to export sub-system for refinement. Then in a bottom-up flow, the IP integrator can import and update complex IP bundles into SoC design and is guided through the configuration, implementation, and verification of the IP.

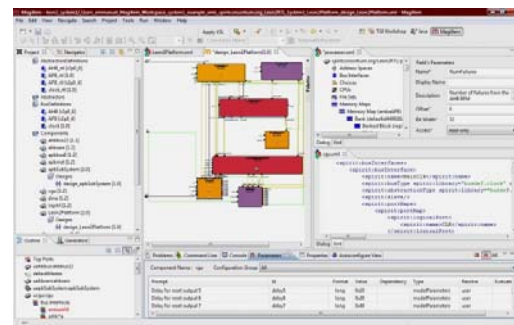


« One Platform, no hassle »

A correct-by-construction methodology and Design Rule Checkers ensure a high quality of the system and compliance with IP-XACT syntax and semantics. In addition requirements traceability features ensure the correctness with certification in Aeronautics (DO-254).

MPA is the main stakeholder of all Magillem solutions. It can be used as a stand-alone platform for assembling and interconnecting IP or in conjunction with the complete Magillem package to offer a high value and comprehensive solution, MPA performs best in association with MIP to build an IP-XACT library by importing and packaging components, MGS to introduce custom automation to the platform under construction using generators, and MRV to manage the software interface (registers and memory).

Features



- Digital, Analog, mix and System platform viewer
- Version and configuration management
- Certification requirements traceability
- Verification tool kit
- Checkbox Interface to connect IP (bus, signal, split, tie)
- Drag and drop IP into design
- Various EDA tools connectors
- RTL and ESL Netlister
- Verification tool Kit

Benefits

To the HW System architect Engineer:

- Fast architecture Exploration and definition

To the IP provider:

- Package IP in a reusable format that will guide the IP integrator through the configuration, implementation, and verification

To the IP integrator:

- Heterogeneous architecture integration
- Easy configurable and reusable IP library management
- Auto Generation of ESL/HDL code

To the Project lead:

- Synchronization of collaborative work, verification, tracking, reporting

To the verification Engineer:

- Fast verification of the HW implementation of IP
- Validation plan and coverage scoring
- Easy monitoring, configuration and initialization



Mining your own expertise



Specifications

MPA FEATURES	Premium	Platinum
IP-XACT v1.0, v1.2, v1.4, v1.5 support	X	X
IEEE 1685 support	X	X
Component and Design Rules Checker		
Digital Rules	X	X
Analog Rules		X
Support for Custom Rules	X	X
IP-XACT (all versions) Rules Support	X	X
IEEE 1685 Rules Support	X	X
Hierarchical Netlister		
VHDL IEEE 1076	X	X
Verilog IEEE 1364	X	X
SystemC IEEE 1666, with automatic shell generation for VHDL and Verilog IPs (IUS, Questa)		X
VHDL-AMS IEEE 1076.1		X
Verilog-AMS LRM 2.3.1		X
SystemC-AMS LRM 1.0		X
SystemVerilog IEEE 1800		X
Graphical Edition		
System graphical front-end editor	X	X
Analog graphical front-end editor		X
IP browser	X	X
Parameters view (all/filtered)	X	X
Dynamic Hierarchy view	X	X
Component Generator launcher	X	X
Miscellaneous Automated operations		
Merge, Flatten, Move operation	X	X
Virtual Hierarchy Management	X	X
Component Stubbing operation	X	X
Publish/update platform		X
Statistic reporting	X	X

MPA FEATURES	Premium	Platinum
EDA Tool Connectors		
IC and system simulation		
Modelsim connector (Mentor)	X	X
Incisive connector (Cadence)	X	X
VCS connector (Synopsys)	X	X
ESL synthesis		
Catapult C connector(Mentor)		X
C-to-Silicon connector(Cadence)		X
IC synthesis		
Design Compiler connector (Synopsys)		X
Encounter RTL compiler (Cadence)		X
FPGA synthesis		
ISE connector (Xilinx)	X	X
Quartus II connector (Altera)	X	X
Sinplify connector (Synopsys)	X	X
Precision connector (Mentor)	X	X
Analog IC simulation		
HSpice & Eldo connector		X
Virtuoso connector (Cadence)		X
Database		
Cadence OpenAccess		X
Legacy design import		
Import VHDL design to IP-XACT	X	X
Import Verilog design to IP-XACT	X	X
DO254 support		X

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