



Magillem Register View

Description

Entering the market with a product targeting the traditional need of IC designers to manage the Registers, MAGILLEM is offering a brand new approach: Customers do not have to choose between an Excel based Register capture system, disconnected from their design, or an expensive, dedicated Register management tool, still not addressing the issues of collaborative work. Cost effective, and non-compromising, MRV by Magillem offers a Register View of IP-XACT Systems and IPs:

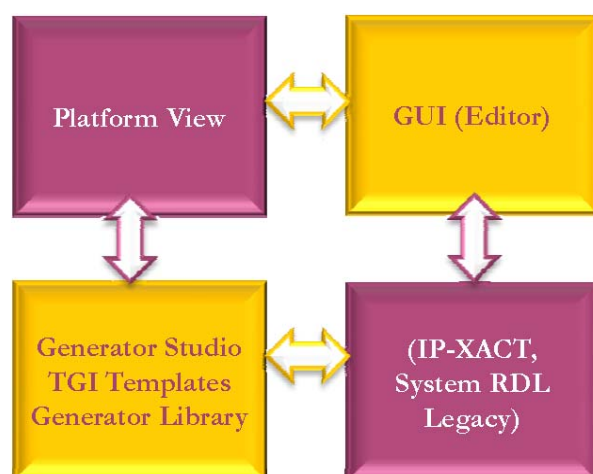
- Advanced Parameterization, Reuse and **Collaborative** strengths to describe Modal **Hierarchical** Components, Registers and Memory-Maps
- Powerful Data **Coherency** and **Synchronization** built-in Engine ensuring at the earliest stage correct-by-construction register-oriented IP and SoC views
- Flexible Generators Customization performed thru native Object Oriented API, template-based Engine or IP-XACT TGI
- Zero learning curve GUI with graphical editors allowing for the fast capture of registers and memory maps, IP-XACT (robust but tedious) is hidden behind comfortable designer-oriented capture graphical interface.
- Leading-edge Textual Input Language compliant with state-of-the-art Magillem, Eclipse and IP-XACT Technologies

MRV supports the hierarchy in IP-XACT: base address and offset can be defined as configurable elements.

One can flatten or keep the hierarchy (no duplication of the memory related xml tag inside a top component). This is essential when a platform becomes an IP and the IP owner wants to make a deliverable.

In the IPXACT description, the system will contain a pure hierarchical component with only a pointer to a design or a flattened component with a full copy of the memory maps from the component leafs.

Architecture

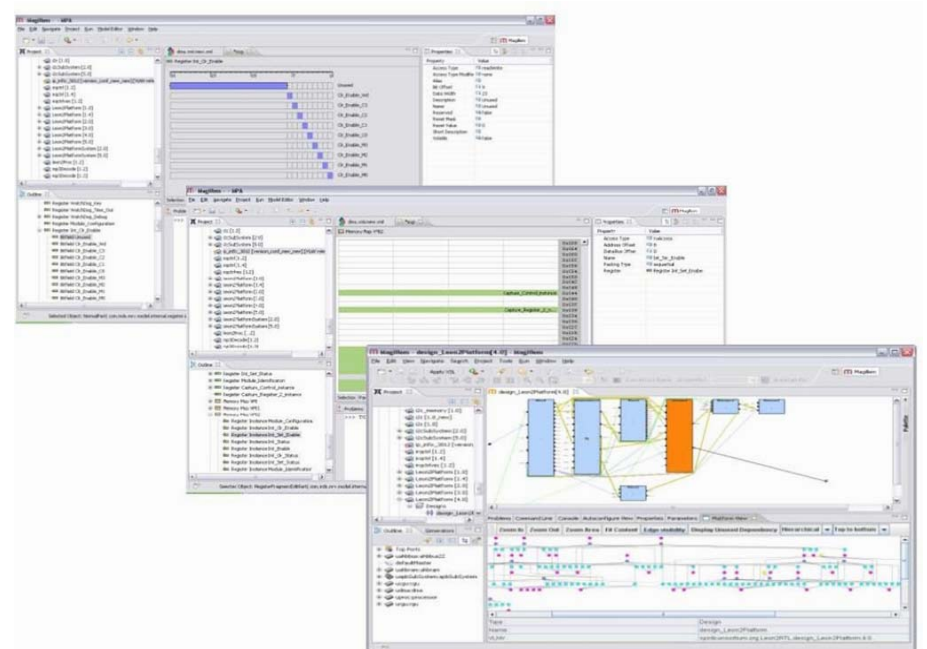


« Capturing Registers, but for a cause »

MRV supports both modes. In a bottom up approach we are building a complete view of the system. The declared relationships between the levels, the instances and the dependencies are preserved. We provide a full TGI support to write generators. So if you want to create an API on top of the TGI, it is easy.

Design Rule Checks are performed to ensure the correctness of the component description against the official IP-XACT syntax and semantics but focused on the memory, register and bit field organization.

Features



- Complete Register and Bitfield editor
- Move and resize Bitfields
- Memory Map editor
- System Memory Map Editor
- Drag and drop inside the memory map
- Copy/Paste
- Visual identification of overlaps
- True synchronization with RTL or ESL platform
- True Hierarchical description

Benefits

To the Specification Owner:

- Fast checking/verification of the HW implementation of the register specification
- Redesign is simplified
- No learning curve, no knowledge of IP-XACT

To the HW engineer IP level:

- Auto Generation of HDL code

To the HW engineer System level:

- Auto Generation of HDL code

To the System level SW engineer:

- Coherency

To the Project lead:

- Synchronization of collaborative work, verification, debug



Mining your own expertise



Specifications

MRV FEATURES	Basic	Premium	MRV FEATURES	Basic	Premium
Import / Export			Generators		
IP-XACT v1.0, v1.2, v1.4, v1.5	X	X	Verilog and VHDL Headers		X
IP-XACT IEEE 1685	X	X	Verilog and VHDL Bus Interface & Register Blocks		X
Register Description Language		X	Verilog and VHDL Interconnect (AMBA AHB, APB...)		X
EXCEL, CSV format	X	X	Verilog and VHDL Testbench		X
Support for Importing/Exporting Custom Formats	X	X	SystemVerilog		X
Register & System Management			SystemC TLM		X
GUI with Linting Cross Checking Editor	X	X	Vera		X
TRUE graphical Editor	X	X	Cadence VRAD for eVC		X
IP Memory Map Capture & Management GUI	X	X	Cadence Vplan		X
TRUE synchronization with RTL platform		X	HW and SW Documentation (RTF Format)	X	X
TRUE synchronization with ESL platform		X	HW and SW Documentation (HTML Format)	X	X
System Memory Map Capture & Management GUI	X	X	HW and SW Documentation (PDF Format)	X	X
Register Description Language		X	HW and SW Documentation (Frame Maker Format)		X
Database Differencing GUI	X	X	Datasheets Documentation (HTML)		X
Database Differencing CLI	X	X	Datasheets Documentation (PDF)		X
System Level Schematic Configurability	X	X	Assembly Header		X
Customizable Data Structure Format	X	X	C-code Headers		X
Design Rule Check			C++/SystemC Header	X	X
Standard Rules	X	X	C-code HW Access Functions (HAL)		X
Support for Custom Rules		X	C++/SystemC HW Access Classes(HAL)		X
DRC GUI	X	X	C-code Integration Tests		X
DRC CLI		X	Basic RTOS Framework		X
Rules Design Application		X	Operating Systems Supported		
Rules Management Application	X	X	Linux	X	X
SPIRIT Rules Support	X	X	Windows 2000/XP	X	X
Generation					
Generator Configuration & Run GUI	X	X			
Generator Configuration & Run CLI	X	X			
Generator Specific Rules		X			
Customizable Generators		X			
Generator Customization GUI		X			

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