

Master & Slave AMBA AHB / VCI bus wrappers



Description

The Master and Slave AMBA AHB bus wrappers are used to connect bus independent Intellectual Properties (IPs) to an AMBA AHB bus controller. They let system designers seamlessly integrate VCI compliant IPs in their system core, enabling a practical reuse methodology.

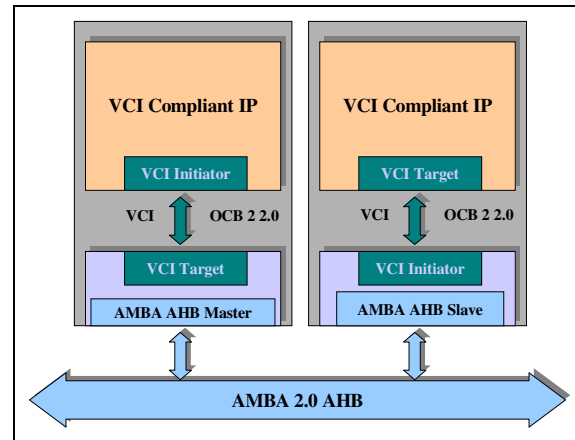
Two versions of the wrapper are available, one for masters and another for slaves. They both manage burst transfers in order to increase the bus throughput.

If asynchronous clocks are used for an IP and the bus controller, dedicated logic can be inserted to match the two clock domains.

The master wrapper can deal with RETRY or SPLIT responses given by the slave wrapper or any other slave connected to the bus.

IP Deliverables :

- Synthesizable VHDL code with generics for different configurations.
- Customized Validation platform
- User's Manual
- Synthesis Scripts
- Integration Support



Features

- AMBA AHB bus master wrapper to connect a Basic VCI initiator
- AMBA AHB bus slave wrapper to connect a Basic VCI target
- The master wrapper supports RETRY and SPLIT responses
- The slave wrapper can generate RETRY or SPLIT responses
- Manages asynchronous clocks

Technical Specifications

- AMBA AHB rev 2.0 compliant (fully tested with Verity's AHB eVC)
- VCI OCB 2.2.0 compatible

Supported Technologies

- Design for high performance ASIC/PLD/FPGA system

Availability

- Now

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