

Multi Channel SDR SDRAM Memory Controller



Description

The Memory controller is used to interface a SDR memory to an AHB, OCP or BVCI host system core, which doesn't have an internal SDR controller. Several subsystems (N) can share the same controller. Each bus channel can be configured separately with asynchronous clocks management. This controller includes an AMBA APB port for configuration management.

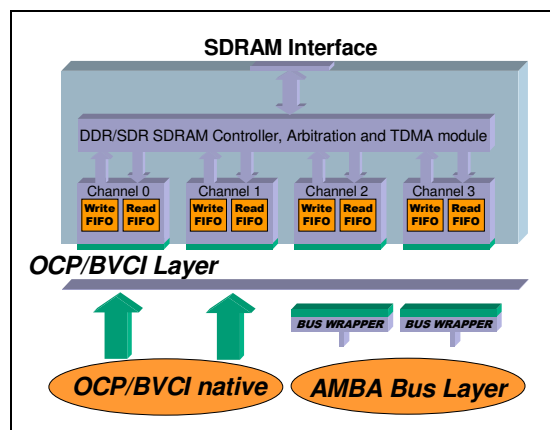
The memory controller may have 1 to N channels. The input fifo size, for the write buffer and the read buffer, becomes a parameter to increase the global system performance. The memory controller arbitration schemes are based on fixed priority or round robin algorithm but it is possible to add a third party algorithm. A TDMA module is added over the arbitration scheme, so that you can introduce QoS between the channels.

The memory controller core is based on BVCI or OCP for the interfaces, with optional wrappers to adapt to bus protocols (e.g. AMBA, CoreConnect). A direct BVCI or OCP connection is proposed with or without asynchronous management to reduce the port access latency. A dedicated "High Speed Port" is included to optimise the SDR bandwidth, useful for DMA interfacing.

IP Deliverables :

- Graphical assistant for generating synthesizable VHDL code depending on memory configuration.
- Customized Validation platform
- User's Manual
- Synthesis Scripts.
- Integration Support

Email: contact@magillem.com
Web: <http://www.magillem.com>



Features

- Multi channels with AMBA AHB, BVCI or OCP Slave Interface
- AMBA APB Slave or BVCI Interface for SDR controller configuration
- Compliant AMBA AHB split capable
- Tools for Performance analysis

Technical Specifications

- Support SDR Memory specification
- Fixed burst length memory transfers
- Programmable SDR data width and address width
- Automatic memory Refresh/Initialization and programmable memory timing characteristics
- Asynchronous clock management on every channel
- Channel Arbitration with several algorithms and TDMA module

Supported Technologies

- Design for high performance ASIC and FPGA systems

Availability

- Now