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Magillem Releases its Verification Solution to Complement Its Existing Suite of Tools

A unique methodology to drive the verification process through a build-in toolbox cockpit

PARIS / NEW YORK, NY, July 27 2009 – Magillem the world leader in IP-XACT methodology tools today announced the availability of Magillem Verification Solution (MVS) to solve the verification complexity and bottleneck problem.

Functional verification is taking an increasingly significant place in the design cycle. Verification of complex functionality integrated with new design tools poses an on-going challenge in global product cycle reduction. MVS delivers a complete seamless verification methodology to fill this need and integrated in the Magillem suite of tools as follows:

- The *Magillem Platform Assembly* provides an intuitive graphical interface to design and configure the verification platform that will stress the Design Under Test (DUT), testing all the different cases defined by the verification plan. Adding Verification IP to the platform allows the DUT to be driven and monitored from a verification cockpit. The interoperability and consistency between models of different abstraction levels allows the possibility of switching from a system configuration to a Hardware Description Language (HDL) configuration.
- The *Magillem Generator Studio* provides a set of specific plug-and-play generators for performing automatic monitoring, configuration and initialization steps.
- The *Magillem Verification Solution* provides a unique methodology for step-by-step, error free verification of IP integration and comparison of results with a golden reference. The MRV product displays the complete memory and register map at all stages of the verification scenario.
- Finally the *Magillem Platform Assembly* allows import and export of the verification plan to achieve sign-off coverage and track the progress with time, in accordance with the objective, in a dedicated and customized view. This metric driven verification management system provides up-to-date information on the status of the verification.

"We are introducing an integrated methodology for SoC design and verification build around a solid backbone using robust tools and open Standards. A SoC is really ready to be shipped when the complete software application works correctly and completely. The Magillem Verification Solution gives a new way to capture both HW and SW activities, helping teams organize the SoC verification. MVS allows the support of multiple industry standard modeling languages and provides a virtual board system description enabling pre-silicon software development, analysis, and verification." says Cyril Spasevski, CTO at Magillem.

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About Magillem

Magillem provides customers with tools and services that drastically reduce the global cost of complex design, help them preserve their independence from EDA vendors and their investment by relying on a worldwide adopted Xml format: IP-XACT by the SPIRIT Consortium™ (soon to be IEEE 1685) to which Magillem is a key contributor. Clients are semiconductors manufacturers (ASICs, ASSPs), system integrators and information technology companies engaged in the research, design, development, manufacturing and integration of advanced technology systems and products (using ASICs and FPGA).

The headquarters are in Paris, France with a subsidiary in the USA and sales office in Asia.

