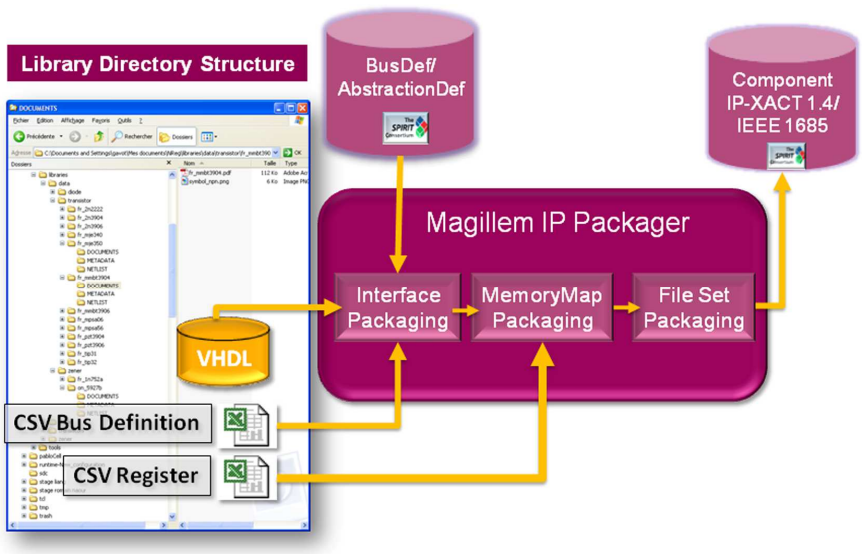
m Ip-Xact Packager

to index your IP repository in a pivot IEEE format

Description

Efficient migration to an IP based methodology and flow first requires capture of legacy IP libraries in a technology independent format, using an easy-to-use, scalable and automated process. Magillem IP-XACT Packager automatically creates an IP-XACT certified description for any VHDL, Verilog or SystemC IP using a non-intrusive technology to your existing flow. The packager scalability enables automatic import of legacy component libraries and its high level of modularity facilitates smooth integration with any client directory structure, with support of customer specific information. Magillem IP-XACT packager advantages are:

- ✓ Non-intrusive, scalable and automatic process for legacy and new IPs.
- ✓ Proven methodology enabling seamless packaging of IP client portfolio.
- ✓ Support any kind of IP description, client data structure and input information, through a highly configurable process.
- ✓ The packager scalable architecture also enables automated re-capture of a library of components following input changes
- ✓ Full or incremental packaging
- ✓ Support of all IP-XACT formats.
- ✓ IP-XACT compliance and data consistency ensured by construction and assessed with built-in Magillem IP-XACT checkers suite.
- ✓ CAD flow independence.



Magillem IP-XACT Packager can plug to various client infrastructures:

- Directory structure:
  - CoReUse™
  - Client specific structure.
- Direct links to revision control systems: CVS, SVN, Clearcase, DesignSync

Features

IP Capture

RTL Import

As a major Contributing Member of the Spirit/Accellera Consortium, Magillem has a proven experience with IP-XACT usage. Magillem IP Packager can target any IP-XACT version:

- Legacy IP-XACT versions: 1.0, 1.1,1.2, 1.4
- IEEE1685 standard.

Magillem Packager relies on Magillem Checker Suite that guarantees the validity of generated files against IP-XACT grammar, semantics and the Spirit/Accellera Consortium guidelines. Magillem Packager is able to capture from the following formats:

- VHDL ‘87, ’93.
- Verilog ’95, ’01
- SystemC 1.x, 2.x, TLM 1.x, TLM 2.x.
- DITA 1.0, 1.1, 1.2
- Any CSV or Excel spreadsheet can be imported with a GUI, assisting the translation to/from IP-XACT

Magillem Packager can also create IP-XACT descriptions for mixed VHDL/Verilog hierarchical components defined in different HDL libraries. Advanced RTL import allows importing structural RTL into a valid ip-xact design.

The following language extensions are also supported, with Magillem AMS Solution:

- VHDL-AMS : IEEE 1076.1
- Verilog-AMS : LRM 2.3.1
- SystemC-AMS: LRM 1.0.

Services proposed by Magillem experts on IP Packaging are:

- Audit of the existing libraries, and definition of the most efficient import strategy.
- Tool customization to handle customer specific information and integration with the client infrastructure.

Benefits

To the IP provider:

- Define an IP in a reusable format that will guide the IP integrator through the configuration, implementation, and verification
- Produce a correct by construction IP-XACT description, without requiring IP-XACT expertise

To the IP integrator:

- Heterogeneous architecture integration
- Easy configurable and reusable IP library management

To the Project lead:

- Synchronization of collaborative work, verification, tracking, reporting

“If I'd known how much packing I'd have to do, I'd have run again”

Harry S. Truman

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Specifications

Magillem IP-XACT Packager Features	Premium	Platinum
IP-XACT 1.0, 1.2, 1.4 support	X	X
IP-XACT IEEE 1685 support	X	X
Compliance checks		
Syntax checks	X	X
Standard IP-XACT and additional Magillem semantic checks	X	X
Directory structure support		
CoReUse™ standard repository structure	X	X
Custom repository structure	X	X
Packaged information		
IP interfaces and parameters from source entity/module	X	X
Bus interface definitions from TCL commands or CSV format	X	X
Complete File set creation (mixed vhdl/Verilog) of a component view and its dependencies	X	X
MemoryMap elements (blocks, registers, fields, enumeration, uvm standard extensions)	X	X
IP-XACT views	X	X
Supported HDL languages		
VHDL'87, '93	X	X
Verilog'95, '01	X	X
SystemC 1.x, 2.x		X
VHDL-AMS IEEE 1076.1		X
Verilog-AMS LRM 2.3.1		X
SystemC-AMS LRM 1.0		X
Hierarchical HDL import		
Structural HDL netlists	X	X
Structural HDL VHDL, Verilog (packages, function, include file, pragmas supported)		X
Editors		
IP-XACT editors (all ip-xact versions)	X	X
BlockForge		X
Customer Specific information Import		
Register and memory map definition: CSV, Excel, FrameMaker, SystemRDL	X	X
Legacy XML	X	X
Documentation, DITA	X	X
Design rules integration	X	X
Protocol coverage rules	X	X
Integration with revision tools		
CVS/SVN connectors	X	X
Clearcase/DesignSync connectors	X	X
Scripting		
Command line interface, TCL + python console, TGI generators (with MGS token)	X	X
Platforms	X	X
32bit : Windows XP, Vista, 7, Linux RHE4, RHE5	X	X
64bit : Windows XP, Vista, 7, Linux RHE4, RHE5		X

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