

Description

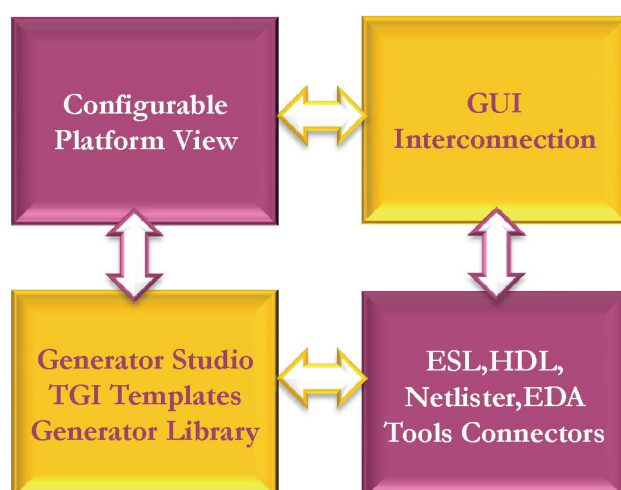
To accelerate the design of complex systems, such as System-on-Chip (SoC), and FPGA based solutions, ESL virtual platform, the IP-XACT standard provides a mechanism for describing and handling multi-sourced IP that enables automated design integration and configuration within multi-vendor tool flows.

To achieve these goals, Magillem presents MPA as the center piece of a powerful intuitive, Integrated Design Environment. The user friendly interface guides the designer during platform assembly and configuration, and streamlines exploration and implementation of IP-based systems:

- A complete graphical platform editor providing advanced parameterization, reusable methodology and collaborative features
- A digital and/or analog design environment (editor, DRC, library management)
- A set of predefined automated operations to easily connect IP through the hierarchy, handle components (move, merge, flat, insert...) and reduce risks of errors.
- A support of virtual hierarchy allowing the same platform to be hierarchically described according the flow step (power domain, verification, software, team, abstraction level, ...).
- A graphical interface to manage the library of generator, plugins for the Magillem Generator Studio and customize the automation of the platform for dedicated applications
- A large range of connectors to EDA tools (Mentor, Cadence, Synopsys, Xilinx, Altera)
- RTL and ESL netlister (VHDL, Verilog, SystemC, VHDL-AMS, Verilog-A, SystemC-AMS)
- Automated generation of an environment used for verification, integrated with a cockpit to control and monitor the Design Under Test, in order to manage the progress.

MPA is well adapted for the V-cycle methodology used by multi-site design teams. Using a top-down approach, it builds a complete view of the system, with all interconnections, ready to export sub-system for refinement. Then in a bottom-up flow, the IP integrator can import and update complex IP bundles into SoC design and is guided through the configuration, implementation, and verification of the IP.

Architecture

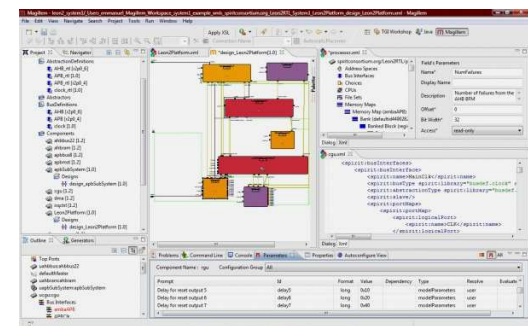


« One Platform, no hassle »

A correct-by-construction methodology and Design Rule Checkers ensure a high quality of the system and compliance with IP-XACT syntax and semantics. In addition requirements traceability features ensure the correctness with certification in Aeronautics (DO-254).

MPA is the main stakeholder of all Magillem solutions. It can be used as a stand-alone platform for assembling and interconnecting IP or in conjunction with the complete Magillem package to offer a high value and comprehensive solution, MPA performs best in association with MIP to build an IP-XACT library by importing and packaging components, MGS to introduce custom automation to the platform under construction using generators, MRV to manage the software interface (registers and memory) and MSE to develop the hardware related software..

Features



- Digital, Analog, mix and System platform viewer
- Version and configuration management
- Certification requirements traceability
- Verification tool kit
- Checkbox Interface to connect IP (bus, signal, split, tie)
- Drag and drop IP into design
- Various EDA tools connectors
- RTL and ESL Netlisters
- Verification tool Kit

Benefits

To the HW System architect Engineer:

- Fast architecture Exploration and definition

To the IP provider:

- Package IP in a reusable format that will guide the IP integrator through the configuration, implementation, and verification

To the IP integrator:

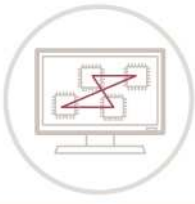
- Heterogeneous architecture integration
- Easy configurable and reusable IP library management
- Auto Generation of ESL/HDL code

To the Project lead:

- Synchronization of collaborative work, verification, tracking, reporting

To the verification Engineer:

- Fast verification of the HW implementation of IP
- Validation plan and coverage scoring
- Easy monitoring, configuration and initialization



Specifications

MPA FEATURES	Premium	Platinum	MPA FEATURES	Premium	Platinum
Native IP-XACT v1.4	X	X	Hierarchy manipulations		
Native IEEE 1685 support	X	X	Merge, Flatten, Move operation	X	X
Component and Design Rules Checker			Virtual Hierarchy Management	X	X
Digital Rules	X	X	Component Stubbing operation	X	X
Analog Rules		X	Publish/update platform		X
Support for Custom Rules	X	X	Design Statistic reporting	X	X
IP-XACT (all versions)+ IEEE1685 Rules Support	X	X	Hierarchical parameter propagation		X
Waiver management on checkers	X	X	TCL / Python / Ruby console	X	X
Hierarchical Netlister			Command line execution	X	X
Configurable header	X	X	EDA Tool Connectors		
VHDL configuration / VHDL package	X	X	IC and system simulation		
VHDL IEEE 1076	X	X	Modelsim/Quarta (Mentor)	X	X
Verilog IEEE 1364	X	X	Incisive (Cadence)	X	X
SystemC IEEE 1666 with automatic wrapper insertion for VHDL and Verilog		X	VCS (Synopsys)	X	X
VHDL-AMS IEEE 1076.1		X	Cadence OpenAccess		X
Verilog-AMS LRM 2.3.1		X	Legacy design import		
SystemC-AMS LRM 1.0		X	Import VHDL design to IP-XACT	X	X
SystemVerilog IEEE 1800		X	Import Verilog design to IP-XACT	X	X
Graphical Edition			DO254 support		X
System graphical front-end editor	X	X	Supported Operating Systems		
Analog graphical front-end editor		X	Linux RHE + Windows 2000/XP/Vista/7 (32bit)	X	
IP browser / IP-XACT editor	X	X	Linux RHE + Windows 2000/XP/Vista/7 (64bit)	X	X
Parameters view (all/filtered)	X	X			
Dynamic Hierarchy view	X	X			
Component Generator launcher		X			
BlockForge editor	X	X			

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