m Register Engine

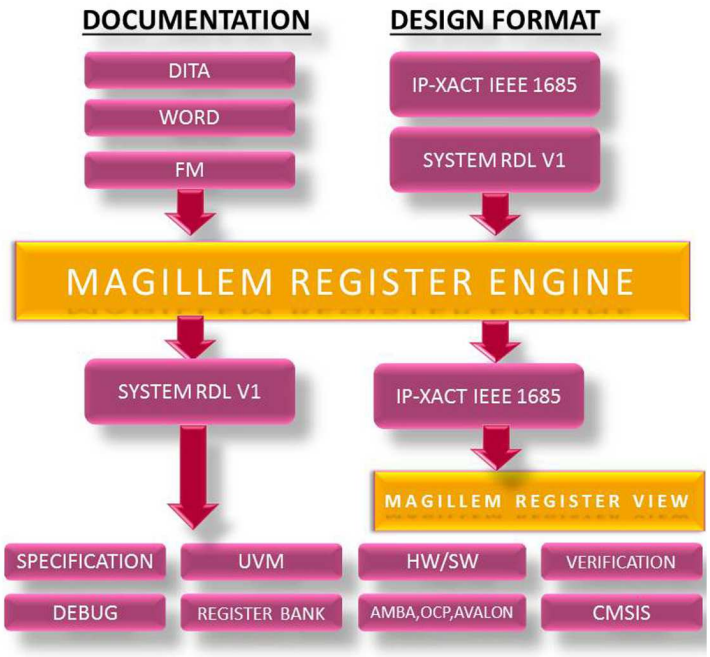
develop, elaborate and compile Register Descriptions using SystemRDL

Description

The register specifications of a complete IP Portfolio or an SOC need to be defined using an advanced register description language. However, lack of coherency and poor collaborative management of this register database become a liability in every design group. This is even more critical when several teams are involved at the integration level using different formats of design data.

MRE acts as an **integration Hub for registers**, able to mix various types of register descriptions, such as SystemRDL , Excel spreadsheet, IP-XACT IEEE 1685 xml formats or documentation (DITA, office word, etc.)
Aggregating Register Data, MRE is able to elaborate and compile the system memory map of a full system, or the memory map for an IP Portfolio. The configuration, interrupts, parameters are taken into account to generate the outputs. The tool generates its outputs as a result of the configuration of the system, the value of parameters, and the presence of interrupts.

MRE provides full support for SystemRDL V1.0. Magillem is already committed to the roadmap of the upcoming Accellera SystemRDL V2.0
MRE generates necessary outputs and views for design, verification, documentation, software development, debug and excel tables



Unique Features

IP & SOC

Register Capture

Magillem ensures smooth and rapid replacement of any existing System RDL engines with its MRE tool.
"SystemRDL is designed to increase productivity, quality, and reuse during the design and development of complex digital systems. It can be used to share IP within and between groups, companies, and consortiums. This is accomplished by specifying a single source for the register description from which all views can be automatically generated, which ensures consistency between multiple views.

*A view is any output generated from the SystemRDL description, e.g., RTL code or documentation. These views include the production of IP-XACT descriptions. SystemRDL is used by many teams to tersely capture a human readable and writable description from which the rest of the deliverables are produced"**
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- MRE has an IDE that assists the user to interactively describe registers. The connection of the IDE to the imported database, results in a "correct-by-construction" solution.
- Connected into the imported database.

Benefits

For Architects

- Facilitate editing of file & memory map
- Supporting various formats

For Design Engineers

- Easy to maintain information about registers and memory map
- Collaborative approach fits various strategies

For Verification Engineers

- Register Descriptions stay in sync between teams and projects
- Generates verification files on as needed, "on the fly"

For Firmware Engineers

- Documentation database in Sync
- Generates Board Support Packages for Debug

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Specifications

Magillem Register Engine FEATURES	PREMIUM
IMPORT	**X**
IPXACT import	**X**
SystemRDL V1.0 import (embedded Perl and verilog preprocessing)	
EXCEL/CSV import	**X**
XML import	**X**
IDE	
Syntax highlighting	**X**
UDPs and library management	**X**
UDP driven compilation	**X**
Auto Completion	**X**
CHECKS	
SystemRDL coherency	**X**
EXPORT	
Elaborated System map in IPXACT	**X**
SystemRDL	**X**
API for MRV custom generators	**X**
Magillem Register View (*)	**X**
DISPLAY integration	**X**
COMPLIANT CODE GENERATOR FOR MRV	
✓ *HTML & word Documentation, HAL C, UVM*	**X**
✓ *Altera Avalon, APB, OCP register bank, CMSIS,…*	**X**
Platform	**X**
✓ Eclipse based, supporting Linux and Windows	**X**

(*) requires MRV license.

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