## Multiple benefits:

- Facilitate the (re)use of UVM components and environments by providing a readable and configurable test platform description,
- Increase the test writer productivity by letting him/her focus on sequences and tests,
- Trace the requirements of tests ( coverage and impacts of change requests), and
- Generate automatically the entire UVM environment and simulation build flow after configuration of the test scenario.

Realizing the UVM test bench generation, we increase the productivity of the Verification team :

## UVM Test-bench generation:

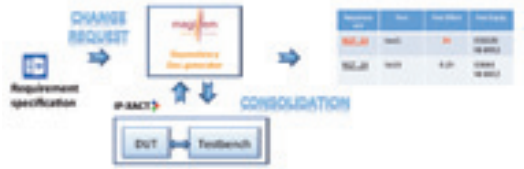
- Simplify the steep learning curve of the UVM architecture
- Save time and help verification engineer to focus on test sequence writing
- Specifying a single source and avoiding tedious and prone error task


## Evaluate the coverage of the requirements:

- Requirements and tests are linked
- Coverage report shows :
  - the r**equirements covered** by the verification flow
  - the latest test execution


## Evaluate the impact of a change request on tests or DUT and identify non-regression test suite:

- A **change request** in the specification can impact test suite, DUT, UVCs ...
- **Impact report** shows **the list of test** involved by a change request or the consolidation of a change request




# Software that streamline your design and documentation flows

magillem

**mining your own expertise**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# Magillem : Requirement based UVM Verification and Traceability

" Generation of UVM compliant Test Benches for Industrial Systems using IP-XACT with UVM-SystemC and SystemC AMS "

magillem

**Sustainable Innovation to drive Industries' Efficiency**

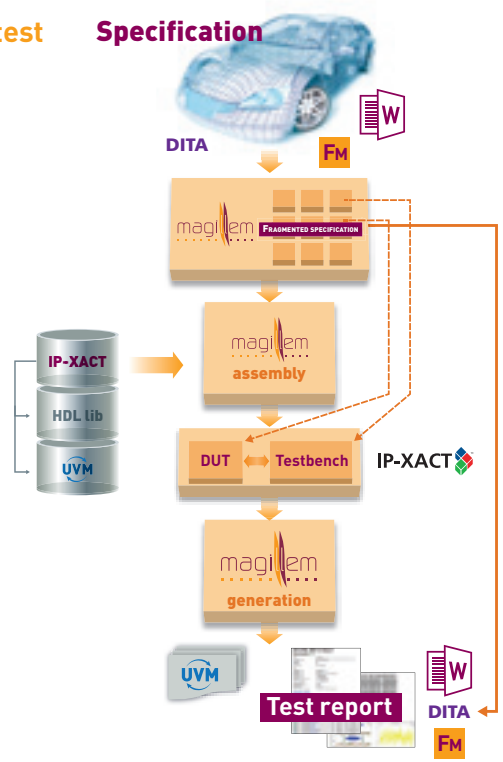
# Magillem:

Generation of UVM(*) compliant Test Benches for Industrial Systems using IP-XACT with UVM-SystemC and SystemC AMS

The complexity of electronic systems is increasing. More and more systems are characterized by having close interaction between embedded software (SW), hardware (HW) and analog components. Furthermore, numerous systems are safety critical systems, and as a consequence, verification of all related requirements is mandatory. Hence the need for a virtual prototype (VP) of the hardware architecture. Using the VP, software engineers are able to debug the HW/SW system before the actual availability of the hardware prototype. Later on, when the HW is available, in the form of an FPGA or test chip, a strong benefit is to reuse the test cases and test benches used for the VP, and to apply them as well to validate the hardware prototype.

## Traceability of test requirements

- **Fragments the Test specification in Minimum Reusable Unit during the import**
- **Builds IP-XACT test-bench**
- **Creates links between fragments and IP-XACT elements of test-bench**
- **Netlists UVM test environment**
- **Traces the test requirements**
- **Analyzes the impact of change request**
- **Generates reports**




(*)The Universal Verification Methodology (UVM), now a state-of-the-art standard, supports design and verification engineers with an open-source class library to create verification components and models for digital test-benches.

## Seamless verification flow based on IP-XACT

**Magillem Platform Assembly tool offers a graphical or TCL scripting interface to compose the IP-XACT platform** and generate the whole UVM-SystemC test environment (in .h and .cpp files) with the different UVM layers (top-level, test and test bench) in the SystemC and SystemC-AMS language.

**The IP-XACT-based verification methodology aims at facilitating** the use of UVM objects by providing a simple, configurable, and readable description of a UVM verification component (UVC), to automate the creation of the test environment.

From a verification point of view, the user builds the UVM platform by selecting the UVCs from an IP-XACT library, and instantiate, configure and interconnect these to build the test bench. Test and top-level are similarly assembled and configured.

The automation is extended by the new traceability concept available in Magillem to permit the execution by a requirement driven verification using tracing down to the test component configuration. Thanks to the stimuli text file driving the test sequence, one can reuse the test scenario definition between the verification and validation phase.

### IP-XACT EXTENSIONS FOR UVM-SYSTEMC

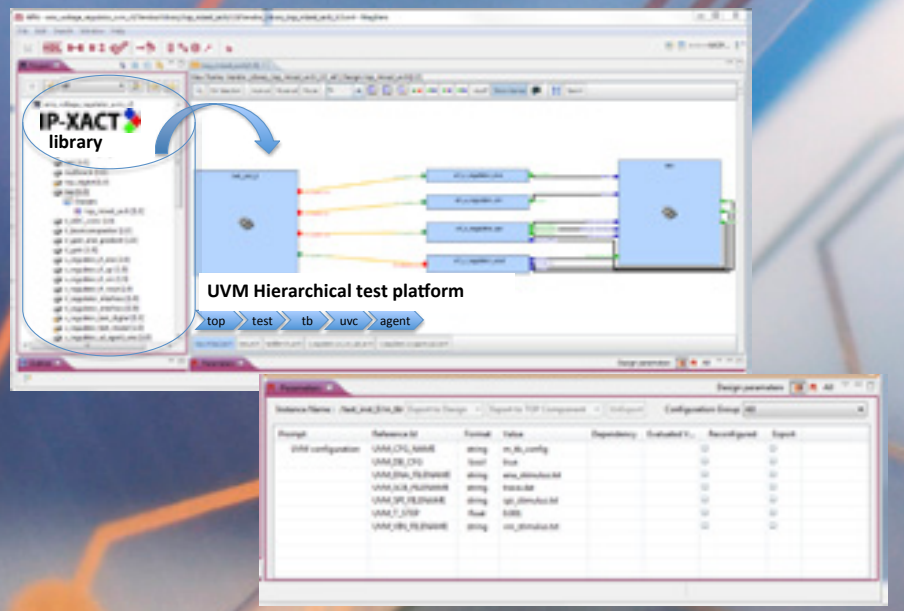
The IP-XACT meta data is used to provide a unified specification for a verification component to exchange and share compatible components from multiple companies or services.

More specifically, the creation of UVM extensions in IP-XACT enable efficient assembly and configuration of test bench, test and top level elements by generating the relevant SystemC and SystemC-AMS views necessary to conduct verification.

The UVM architecture is structured in layers from the top level to the virtual sequencers, and uvcs, which can be reused independently of each other.

To keep this reusability, the IP-XACT description is following the same hierarchical structure using the concept of design, component and hierarchical view defined in the IEEE1685 standard schema.

### Magillem Platform Assembly tool to build the UVM test environment




A parameter dedicated view facilitates the configuration of the platform of test and propagates through the hierarchy the parameter values to the sub-element using the IP-XACT description of the different configuration object associated to their IP-XACT component.