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Contacts:
Kurt Shuler
Arteris IP
+1 408-470-7300
kurt.shuler@arteris.com

Pascal Chauvet
Magillem
+1 415-867-5094
chauvet@magillem.com

Arteris IP and Magillem Partner to Create Integrated System-on-Chip Architecture Environment

Single environment allows design teams to more easily build AI and autonomous driving SoCs using FlexNoC and Ncore IP and share data for ISO 26262 compliance

CAMPBELL, Calif. – June 25, 2018 – Arteris IP, the world's leading supplier of silicon-proven commercial network-on-chip (NoC) interconnect intellectual property (IP), and Magillem, the leading provider of front-end design XML solutions and best-in-class tools to reduce the global cost of complex designs, today announced a partnership and product integration that accelerates the architectural definition of complex chips.

The first technical fruit of the partnership is the validation of full compliance of Arteris IP interconnects with the Magillem environment. Within a single environment, joint customers can now easily build a system-on-chip with multiple Ncore and FlexNoC instances. Using the Magillem front-end design environment (MAI, MPA and MRV), users can import Arteris FlexNoC non-coherent interconnects and Ncore cache coherent interconnects using the IP-XACT format. Detailed descriptions of the Arteris IP NoC instances imported into the Magillem environment can be used for full SoC assembly at the RTL and SystemC levels.

The Magillem / Arteris IP integration will be demonstrated at the Design Automation Conference (DAC), 24-28 June 2018, in the Magillem booth #1351.

This integration eases the design of today's highly complex artificial intelligence (AI) and autonomous driving SoCs, which are now bounded by the performance of on-chip interconnects rather than the performance of on-chip processors and hardware accelerators. The integration enables automatic checking and synchronization of system memory maps and speeds up the creation of derivative chip designs. Furthermore, use of machine-readable IEEE IP-XACT data allows for automated traceability throughout the development flow, which is important for compliance with functional safety standards like IEC 61508 and ISO 26262 for automotive systems.

"The Magillem integration with Arteris FlexNoC and Ncore interconnect IP enables not only the easier design of highly complex systems-on-chip, but also more efficient and automated

information sharing between IP providers, semiconductor vendors, ISMs and systems houses," said Isabelle Geday, Magillem CEO.

"Our integration with Magillem makes it easier for our joint customers to create state-of-the-art AI and autonomous driving chips and maintain accurate documentation of chip information throughout their lifecycles," said K. Charles Janac, President and CEO of Arteris IP. "This is especially important for mission critical SoC designs that must meet the IEC 61508 and ISO 26262 functional safety standards."

About Magillem

Magillem has been the pioneer, since 2006, in software leveraging business content for top tier semiconductors and embedded systems accounts worldwide. Magillem has been listed on Euronext Paris since 2009 (FR0010827741) and is trusted by numerous clients like Altera, Samsung, Qualcomm, NXP, ST Microelectroni*cs, Texas Instruments, Thales.*

Magillem has 60 employees, including 48 engineers and PhDs in Research & Development alone. With an office in Tokyo, a subsidiary in Korea, one in China, 3 agencies in the United States (New York, Austin and the San Francisco Bay area) and 8 distributors in Asia and Israel, its footprint extends to all major countries. For more information, please visit www.magillem.com

About Arteris IP

Arteris IP provides network-on-chip (NoC) interconnect IP to accelerate system-on-chip (SoC) semiconductor assembly for a wide range of applications from automobiles to mobile phones, IoT, cameras, SSD controllers, and servers for customers such as Samsung, Huawei / HiSilicon, Mobileye (Intel), Altera (Intel), and Texas Instruments. Arteris IP products include the Ncore cache coherent and FlexNoC non-coherent interconnect IP, the CodaCache standalone last level cache, as well as optional Resilience Package (ISO 26262 functional safety) and PIANO automated timing closure capabilities. Customer results obtained by using the Arteris IP product line include lower power, higher performance, more efficient design reuse and faster SoC development, leading to lower development and production costs. For more information, visit www.arteris.com or find us on LinkedIn at https://www.linkedin.com/company/arteris.

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