m Register View

Collaborative work on Register View of systems and IPs

Description

MAGILLEM presents a brand new approach targeting the traditional need to manage registers for System-on-chip solutions: customers no longer have to choose between Excel based Register capture, disconnected from their design, or an expensive, dedicated Register management tool, which still does not address the issues of collaborative work and management of IPs/sub-systems delivered by separate teams and third party companies. Cost effective, scalable, and non-compromising, MRV by Magillem offers a Register View of Systems and IPs, based on IP-XACT standard, which addresses today's challenges of HW/SW integration in complex chips:

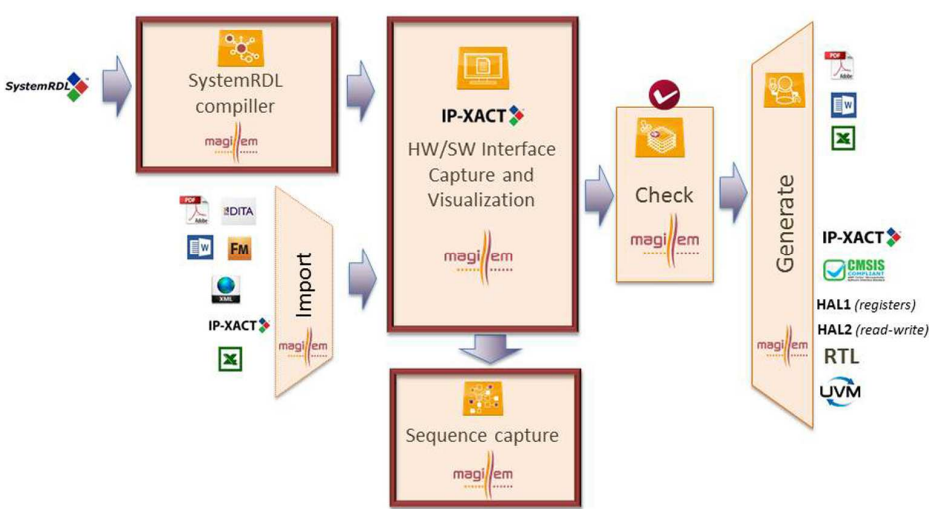
- Integration of configurable IP register descriptions (containing thousands of registers), delivered by multiple different vendors, in a hierarchical system
- Import and capture of register descriptions defined in different formats (CSV, Excel, XML…) into a single database
- Reduce errors and misalignments thanks to synchronized database and comprehensive consistency checks
- Tight link with HW interface definitions and platform connectivity, to generate correct and aligned system map definitions for SW development
- Tool and register description format independence, thanks to IP-XACT standard, now IEEE1685 (native format supported by Magillem environment)

Magillem Register View is at the meeting point of SW, HW and the documentation flows, providing different connection with Magillem tools:

- the Sequence Editor (MSE) that uses the register descriptions,
- the Platform Assembly (MPA) that describes the architecture of the system,
- the Content Assembly (MCP) to generate documentation used by the different teams (architect, software, design hardware and verification).

The data model and GUI provide efficient capture, import and export required to address the register complexity (50-100k Registers) of current systems and integrate seamlessly with any client legacy format. The solution is proven in production and is scalable to work efficiently regardless of the number of registers captured.

Architecture



Features

Embedded SW

- Import of register/bit fields description from CSV, Excel, DITA, CMSIS or FrameMaker formats with the possibility to customize import from client legacy CSV, Excel or other documentation formats
- Zero learning curve GUI with graphical editors enabling fast viewing and capture/modification of registers and memory maps. IP-XACT syntax is hidden behind intuitive designer–oriented graphical interface.
- Advanced Parameterization including configurable and conditional properties, custom specific access types, register modes, types and hierarchical properties
- Merge/Flatten of IP memory Map definition enables easy update/manipulation/creation of new global memory map for a sub-system or SoC
- Diff/update mechanism enables incremental design flow, collaborative work coherency and synchronization register-oriented IP and SoC views
- TCL API available to script import/export of register/bit fields descriptions and to execute automated generation
- Comprehensive Generator Library natively integrated (in MRV Premium version) in open source edition: generation of HAL API, documentation, System RDL, VRAD, RTL register bank and UVM register model synchronized with RTL (naming convention, backdoor), ...
- Flexible Generator Customization performed through native Object Oriented API, in user-friendly Template environment editor.
- Integrated Design Rule Checks for syntax and semantic errors detection, with on-the-fly markers and contextual resolution help

Benefits

- **Reduce tedious and error-prone tasks** by automated generation of multiple and customizable output formats
- **No learning curve** thanks to intuitive yet powerful and extensible register editor GUI
- **Produce** a correct by construction **IP-XACT** description, without requiring IP-XACT expertise
- **Seamless integration** in existing flows thanks to customizable importer/exporter/register property definitions
- Ensure **synchronization** between **HW, SW and documentation databases**

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Specifications

Magillem Register View FEATURES	Basic	Premium
Import / Export		
IP-XACT 1.0, 1.2, 1.4	X	X
IP-XACT IEEE 1685	X	X
TCL API		X
EXCEL, CSV, DITA, CMSIS, FrameMaker	X	X
Support for custom formats Import/Export	X	X
Register & System Management		
GUI with Linting Cross Checking Editor	X	X
TRUE graphical Editor	X	X
IP Memory Map Capture & Management GUI	X	X
Synchronization with RTL platform		X
Synchronization with ESL platform		X
System Memory Map Capture & Management GUI	X	X
TCL API		X
Database Differencing GUI	X	X
Database Differencing CLI		X
System Level Schematic Configurability	X	X
Customizable Data Structure Format	X	X
Design Rule Checks		
Standard Rules	X	X
Support for additional Custom Rules		X
DRC GUI	X	X
DRC CLI		X

Magillem Register View FEATURES	Basic	Premium
Design Rule Checks		
Rules Design Application		X
Rules Management Application	X	X
IP-XACT Rules Support	X	X
Linux RHE, Windows 2000/XP/Vista/7 (32bit)	X	X
Linux RHE, Windows 2000/XP/Vista/7 (64bit)		X
Supported Operating Systems		
Linux RHE, Windows 2000/XP/Vista/7 (32bit)	X	X
Linux RHE, Windows 2000/XP/Vista/7 (64bit)		X
Generators		
Verilog and VHDL Register Banks (AMBA, OCP, Avalon)		X
UVM Register package (1.0, 1.1, 1.2 and coverage model)		X
register abstraction layer in Specman/e language (VRAD)		X
System RDL		X
HW/SW Documentation (docx Format)	X	X
HW/SW Documentation (HTML Format)	X	X
C-code HW Access Functions (HAL layer 1, layer 2)	X	X
C-code HW Verification Functions (HAL layer 3)		X
ARM® CMSIS-SVD (1.0, 1.1, 1.2)		X
Generator Configuration & launch GUI	X	X
Generator Configuration & launch CLI		X
Generator Specific Rules		X
Customizable Generators		X
Generator Customization GUI		X

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