

Platform Level Design and SoC Verification using IP-XACT

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Abstract— In this tutorial Magillem will introduce its advanced SoC design, verification and flow automation solutions based on IP-XACT. IP-XACT is a XML schema, standardized in IEEE Std 1685-2014, that defines and describes electronic components and their designs, complemented with a generator interface for design and flow automation. By means of several case studies, this tutorial will show how the unique capabilities of the IP-XACT standard, which are beneficial for Platform Level Design. In addition, the usage of IP-AXCT for SoC verification is presented.

Keywords—IP-XACT, IEEE 1685-2014, System integration, SoC verification, UVM, RTI

I. TUTORIAL CONTENT

Are you interested in using IP-XACT, but without looking at XML files and screens? Today, Magillem will expand your interest to new ways of leveraging IP-XACT in SoC design and verification flows. And, of course, without the need for editing XML files yourself.

By means of several case studies, this tutorial will show how the unique capabilities of the IP-XACT standard, which are beneficial for Platform Level Design.

As IP-XACT covers a wide range of applications in the SoC development flow, the application of IP-XACT in the scope of SoC verification is explained next. It will show how the previously presented concepts play a key role in two different SoC verification methodologies:

- An industrial case from NXP will presented the Reusable Test Infrastructure environment. This NXP proprietary environment provides a fully automated SystemC/RTL based verification environment builder. Leveraging most of the IP-XACT capabilities in this area, and being use for years in production it demonstrates a unique industrial case study.
- As part of an innovation project of a European industrial consortium, in which Magillem was involved, IP-XACT was used for UVM test bench and register model generation, verification coverage reporting and change impact reporting. It will demonstrate how IP-XACT facilitates the creation of a seamless verification flow covering specification, creation, execution and reporting.

After these two practical use cases, the attendees of the workshop will have a good understanding what can be achieved with IP-XACT already today. As a next step, the tutorial will show a more advanced third use case of IP-XACT, where the schema is used as a pivot description format for a SoC verification flow:

- As part of another European industrial innovation project called ‘OpenES’, a case study will be presented where IP-XACT and its pivot philosophy provides, in a unique way, an Incremental Traceability framework for various properties in embedded system design.

This third use case will illustrate the importance of the IP-XACT standard to be used as a pivot format, allowing to describe and act, build and verify and ultimately track all collaborative intervention on your platform.

About Magillem:

Magillem Design Services provides customers with tools and services that drastically reduce the global cost of complex design, help them preserve their independence from vendors and their investment by relying on a worldwide adopted formats like IP-XACT (IEEE 1685).

Clients are semiconductors manufacturers (ASICs, ASSPs), system integrators and information technology companies engaged in the research, design, development, manufacturing and integration of advanced technology systems and products (using ASICs and FPGA).

Magillem is headquartered in Paris, France with a subsidiary in the USA and sales offices in Asia. The Magillem team has been a contributor to the IP-XACT specification since 2003. Magillem has established partnerships with EDA vendors, alliances with ASICs leaders, universities, and R&D European. For more information, visit www.magillem.com